IEEE VLSI PROJECTS LISTS

PROJECT CODE	PROJECT TITLE
VTVL01	A Low-Power and High-Accuracy Approximate Multiplier With Reconfigurable Truncation
VTVL02	A Practical Energy/Power Reduction Approach for Parallel Decimal Multiplier
VTVL03	Approximate Recursive Multipliers Using Low Power Building Blocks
VTVL04	Efficient Floating Point Arithmetic for Quantum Computers
VTVL05	Self-Repairing Carry-Look ahead Adder With Hot-Standby Topology Using Fault-Localization and Partial Reconfiguration
VTVL06	Two Distributed Arithmetic Based High Throughput Architectures of Non-Pipelined LMS Adaptive Filters
VTVL07	VLSI Architecture of S-Box With High Area Efficiency Based on Composite Field Arithmetic
VTVL08	Design of High Speed 8-bit Vedic Multiplier using Brent Kung Adders
VTVL09	Design Of High-Speed Vedic Multiplier Using Urdhva Tiryakbhyam Sutra
VTVL10	Optimized Hardware Implementation of Vedic Binary Multiplier using Nikhilam Sutra on FPGA
VTVL11	Analysis of 8 bit Vedic multiplier using different full adder techniques